John T. Anderson

Engineering Note

Date: 10/29/98
Rev Date: ~~10/29/98~~1/6/99

Project: MCM Test Board – CFT Axial Board
Doc. No: A981029A

Subject: Interface between microcontroller and helper CPLD

Introduction

The PIC14000 microcontroller provides a variety of functions in the MCM Test Board (and also in the CFT Axial Board – everything here applies to both). However, as it is a simple microcontroller, the I/O is limited. To accommodate the large amount of external RAM and Flash RAM in the system, the microcontroller requires a helper CPLD to take care of various details. This document examines the requirements of the helper CPLD and details the I/O between the microcontroller and its assistant device.

Available Microcontroller I/O

The PIC14000 has three ports with a total of 20 I/O pins. Port A has four bits, whereas ports C and D both have eight. Various pins have to be reserved for board functions as given in Table 1. Note that two bits of port C have a dual function – more on this later.

Port/Pin number	Function	Use in board
A0 (2)	Generic I/O or A/D input	Global analog feedback for analog multiplexer
A1 (1)	Generic I/O or A/D input	Reserved for future use.
A2 (28)	Generic I/O or A/D input	BUSY* semaphore from dual-port RAM
A3 (27)	Generic I/O or A/D input	I2C_SEL output used to select which set of four octal DACs are programmed.
C0 (19)	Bidirectional I/O; may also act as programmable reference output. Can drive LED.	Part of eight bit multiplexed command/data bus.
C1 (18)	Bidirectional I/O; may also act as comparator output. Can drive LED.	Part of eight bit multiplexed command/data bus.
C2 (17)	Bidirectional I/O; can drive LED.	Part of eight bit multiplexed command/data bus.
C3 (16)	Bidirectional I/O; may also be used as timer clock input; can drive LED.	Part of eight bit multiplexed command/data bus.
C4 (15)	Bidirectional I/O; can be used to cause interrupt on change of state. Can drive LED.	Part of eight bit multiplexed command/data bus.
C5 (13)	Bidirectional I/O; can be used to cause interrupt on change of state. Can drive LED.	Part of eight bit multiplexed command/data bus.
C6 (12)	Bidirectional I/O or I^2C serial control bus.	Part of eight bit multiplexed command/data bus.
C7 (11)	Bidirectional I/O or I^2C serial control bus.	Part of eight bit multiplexed command/data bus.
D0 (6)	Generic I/O or I^2C serial control bus	I^2C serial control bus to four octal DAC devices; which four of eight on CFT board controlled by A3.
D1 (5)	Generic I/O or I^2C serial control bus	I^2C serial control bus to four octal DAC devices; which four of eight on CFT board controlled by A3.
D2 (4)	Bidirectional I/O; may also act as comparator output	ADDR_STRB output to helper CPLD.
D3 (3)	Bidirectional I/O; may also act as programmable reference output	TRANSFER_STRB output to helper CPLD.
D4 (26)	Generic I/O or A/D input	DEC_STRB output to helper CPLD.
D5 (25)	Generic I/O or A/D input	CMD_STRB output to helper CPLD.
D6 (24)	Generic I/O or A/D input	CPLD_BUSY input.
D7 (23)	Generic I/O or A/D input	Reserved for future use.

Table 1

Interface Details

The microcontroller has many functions as given in my previous engineering note A980922A (on web at http://d0server1.fnal.gov/users/janderson/Public~1/a980922a.pdf). These various features condense into the following I/O transfers:

1. Place individual words into DPRAM from microcontroller
2. Transfer words from DPRAM into DACs
3. Transfer words from DPRAM and/or microcontroller to analog muxes, MCM digital controls or power controls
4. Transfer blocks of data from DPRAM to Flash RAM
5. Transfer blocks of data from Flash RAM to DPRAM
6. Transfer blocks of data from Flash RAM to FPGAs
7. Perform Flash RAM maintenance functions

Item 1 is simple I/O, but over a large address range. A helper device is required to hold the DPRAM address while the microcontroller reads/writes the data byte. Thus, the helper must contain an **Address Latch.** The microcontroller loads the address latch by asserting an eight bit value consisting of six bits of address and two bits of latch select, and pulsing ADDR_STRB. With four writes a 24-bit address is transferred to the **Address Latch.**

Item 2 requires only the I^2C interface present within the PIC14000; however, to avoid multiplexing the byte-wide data bus with the I^2C interface, the secondary I^2C port is used and an external transmission gate used to select which set of four I^2C devices are controlled. The I2C_SEL signal provides this control.

Item 3 requires that the helper device provide **Decoder** functions. In order to implement this, the same eight-bit data transfer bus is used by the microcontroller as an address bus, indicated by transitions in the DEC_STRB signal. When DEC_STRB changes state, the current value on the eight-bit data bus is interpreted as an address, and loaded into latches in the helper CPLD. The actual data transfer is signaled by the TRANSFER_STRB signal, which causes the correct decoded CE* or WR* signals to be asserted to the power switches, digital control registers or analog multiplexers throughout the board. This TRANSFER_STRB signal is also used to move a byte of data between the microcontroller and the DPRAM. In order to assist with multiple reads or writes to the DPRAM, the **Address Latch** may be set to auto-increment with each TRANSFER_STRB. The BUSY* semaphore from the dual-port RAM is brought into the microcontroller so that if the data transfer collides with 1553 access to the same location (extrememly remote, but possible), the transmission may be retried. The 1553 port is always given precedence over the microcontroller when accessing the DPRAM.

Items 4 through 6 would require many, many transfers if handled directly by the microcontroller, as the Flash RAM blocks are long. Instead, the microcontroller places a CPLD command on the data bus and pulses the CMD_STRB input to the CPLD, which invokes a state machine that performs the requisite block transfer. While the state machine is running the CPLD_BUSY line is asserted, informing the microcontroller that the CPLD should not be disturbed. Since Flash RAM requires a few special data accesses to initiate writing, the CPLD pins which connect to the data bus may become outputs as the state machine asserts the necessary data values to the Flash; while CPLD_BUSY is asserted, the microcontroller tri-states its data bus port to allow the CPLD and/or the Flash and/or the DPRAM to drive the bus.

Similar to items 4-6, item 7 is handled by writing a command to the CPLD and waiting for the state engine to do its work.

CPLD Commands

Although 256 commands are possible to the helper CPLD, in practice only a very few are used, as shown in Table 2.

Command	Function
0x00	No-op
0x01	Zero a sector of Flash Ram.
0x02	Transfer a sector of DPRAM to Flash RAM
0x03	Transfer a sector of Flash RAM to DPRAM
0x04	Transfer Flash RAM to FPGA
0x05	Set Address Latch to Auto-Increment mode
0x06	Set Address Latch to No-Increment mode
0x07 – 0xFF	Reserved.

Table 2

Decoder Functions

The eight-bit data bus can in theory be used for 256 different decodes; in practice, far fewer are required as shown in Table 3. The decode value is written to the CPLD with a transition of DEC_STRB, and the decoded output actually occurs with the TRANSFER_STRB.

Decode Value	Signal line(s) asserted by next TRANSFER_STRB
0x00	None
0x01	Dual-port RAM CE's (RAM read, which dependent on address in address latch)
0x02	Dual-port RAM CE's and WR's (RAM write, which dependent on address in address latch)
0x03	Analog Multiplexer LE's (select feedback channel); data value selects which channel
0x04 – 0x0B	Power Control Switch 0 – 7 latch enable (one per MCM)
0x0C – 0x13	Digital Control Latch 0 – 7 latch clock (one per MCM)
0x14	Clock Controller (LD_EVNT_DLY)
0x15	Clock Controller (WRT_CLK_CTL)
0x16	Clock Controller (CLKCTL_OE*)
0x174 – 0xFF	Reserved.

Table 3

Required CPLD I/O

The various decodes and interfaces to the CPLD require a fair amount of I/O:

- Eight bits of data for the data/command bus
- ~20 bits for the various decodes
- Eight bits for control of the FPGAs (PPA download mode – see the Altera Flex 10K documentation)
- Four strobe inputs from the microcontroller
- One busy flag back to the microcontroller

- 24 bits for the address latch

With about 65 pins of I/O required, a CPLD like the Altera 7128 is a good fit. Most all the I/O will be consumed, but the amount of logic resources used should be well under 50%.

*Update 1/6/99: MCM Test Board Schematic now in layout, has pinout assigned.